J|A|C|S ARTICLES

Published on Web 07/12/2010

High-Performance Solution-Processed Amorphous Zinc−Indium−Tin Oxide Thin-Film Transistors

Myung-Gil Kim, Hyun Sung Kim, Young-Geun Ha, Jiaqing He, Mercouri G. Kanatzidis,* Antonio Facchetti,* and Tobin J. Marks*

Department of Chemistry and the Materials Research Center, Northwestern University, 2145 Sheridan Road, Evanston, Illinois 60208

Received January 22, 2010; E-mail: m-kanatzidis@northwestern.edu; a-facchetti@northwestern.edu; t-marks@northwestern.edu

Abstract: Films of the high-performance solution-processed amorphous oxide semiconductor a-$ZnIn_4Sn_4O_{15}$, grown from 2-methoxyethanol/ethanolamine solutions, were used to fabricate thin-film transistors (TFTs) in combination with an organic self-assembled nanodielectric as the gate insulator. This structurally dense-packed semiconductor composition with minimal Zn^{2+} incorporation strongly suppresses transistor off-currents without significant mobility degradation, and affords field-effect electron mobilities of ∼90 cm^2 V^{-1} s^{-1} (104 cm^2 V^{-1} s^{-1} maximum obtained for patterned ZITO films), with I_{on}/I_{off} ratio ∼10^5, a subthreshhold swing of ∼0.2 V/dec, and operating voltage <2 V for patterned devices with $W/L = 50$. The microstructural and electronic properties of ZITO semiconductor film compositions in the range $Zn_{9-2x}In_xSn_xO_{9+1.5x}$ ($x = 1-4$) and $ZnIn_{8-x}Sn_xO_{13+0.5x}$ ($x = 1-7$) were systematically investigated to elucidate those factors which yield optimum mobility, I_{on}/I_{off}, and threshold voltage parameters. It is shown that structural relaxation and densification by In^{3+} and Sn^{4+} mixing is effective in reducing carrier trap sites and in creating carrier-generating oxygen vacancies. In contrast to the above results for TFTs fabricated with the organic self-assembled nanodielectric, $ZnIn_4Sn_4O_{15}$ TFTs fabricated with SiO_2 gate insulators exhibit electron mobilities of only ∼11 cm^2 V^{-1} s^{-1} with I_{on}/I_{off} ratios ∼10^5, and a subthreshhold swing of ∼9.5 V/dec.

1. Introduction

Today the most common macroelectronic devices are based on amorphous a-Si:H semiconductor technologies.[1] However, there are increasing demands for new materials with superior properties because of the limited performance (carrier mobilities ≤1 cm^2 V^{-1} s^{-1}) and high fabrication costs of a-Si:H circuitry.[1] New semiconductors could enable unconventional products such as printable RFID tags, flexible displays, transparent smart windows, and sensors, to cite just a few examples.[1,2] Among the promising materials are the recently developed thin-film metal oxide semiconductors ZnO, In_2O_3, IGZO, ZTO, IZO, ZITO, etc. These represent a major advance in the quest for materials which could in principle enable practical unconventional optically transparent electronics. To date, thin-film transistors (TFTs) based on these materials exhibit performance metrics superior in many ways to those of conventional a-Si:H based devices.[3−5] Furthermore, electron mobilities >100−1000 cm^2 V^{-1} s^{-1} have been measured for several thin film and single-crystal metal oxide materials by Hall or time-of-flight measurements.[6] Thus, oxide-based TFTs can achieve very large field effect electron mobilities and large current on/off ratios (>10^5). For example, using pulsed laser deposition (PLD) and high-temperature postannealing ($T_{anneal} = 1400$ °C), the Hosono group demonstrated single-crystalline $InGaO_3(ZnO)_5$ (sc-IGZO) TFTs on the amorphous HfO_2 gate dielectric exhibiting electron mobilities ∼80 cm^2 V^{-1} s^{-1}.[4] The processing of these high-temperature annealed sc-IGZO films is, however, not compatible

(1) (a) Mitzi, D. B. *Solution Processing of Inorganic Materials*; John Wiley & Sons, Inc.: New Jersey, 2009. (b) Sun, Y.; Rogers, J. A. *Adv. Mater.* **2007**, *19*, 1897. (c) Reuss, R. H.; et al. *Proc. IEEE* **2005**, *93*, 1239.

(2) (a) Facchetti, A., Marks, T. J., Eds. *Transparent Electronics: From Synthesis to Application*, John Wiley & Sons, Inc.: Chichester, U.K., 2010. (b) Fan, Z.; Ho, J. C.; Takahashi, T.; Yerushalmi, R.; Takei, K.; Ford, A. C.; Chueh, Y.-L.; Javey, A. *Adv. Mater.* **2009**, *21*, 3730. (c) Street, R. A.; Wong, W. S.; Ready, S. E.; Chabinyc, M.; Arias, A. C.; Limb, S.; Salleo, A.; Lujan, R. A. *Mater. Today* **2006**, *9*, 32. (d) Subramanian, V.; Fréchet, J. M. J.; Chang, P. C.; Huang, D. C.; Lee, J. B.; Molesa, S. E.; Murphy, A. R.; Redinger, D. R.; Volkman, S. K. *Proc. IEEE* **2005**, *93*, 1330. (e) Riviere, B.; Viricelle, J. P.; Pijolat, C. *Sens. Actuators B* **2003**, *93*, 531. (f) Lewis, B. G.; Paine, D. C. *MRS Bull.* **2000**, *25*, 22.

(3) (a) Ryu, M. K.; Yang, S.; Park, S.-H. K.; Hwang, C.-S.; Jeong, J. K. *Appl. Phys. Lett.* **2009**, *95*, 072104. (b) Saji, K. J.; Jayaraj, M. K.; Nomura, K.; Kamiya, T.; Hosono, H. *J. Electrochem. Soc.* **2008**, *155*, H390. (c) Choi, C. G.; Seo, S.-J.; Bae, B.-S. *Electrochem. Solid-State Lett.* **2008**, *11*, H7. (d) Wang, Y.-L.; Ren, F.; Lim, W.; Norton, D. P.; Pearton, S. J.; Kravchenko, I. I.; Zavada, J. M. *Appl. Phys. Lett.* **2007**, *90*, 232103. (e) Yaglioglu, B.; Yeom, H. Y.; Beresford, R.; Paine, D. C. *Appl. Phys. Lett.* **2006**, *89*, 062103. (f) Wang, L; Yoon, M.-H.; Lu, G.; Yang, Y.; Facchetti, A.; Marks, T. J. *Nat. Mater.* **2006**, *5*, 893. (g) Hong, D.; Chiang, H. Q.; Presley, R. E.; Dehuff, N. L.; Bender, J. P.; Park, C.-H.; Wager, J. F.; Keszler, D. A *Thin Solid Film* **2006**, *515*, 2717. (h) Hong, D.; Chiang, H. Q.; Wager, J. F. *J. Vac. Sci. Technol., B* **2006**, *24*, L23. (i) Jackson, W. B.; Hoffman, R. L.; Herman, G. S. *Appl. Phys. Lett.* **2005**, *87*, 193503. (j) Miyasako, T.; Senoo, M.; Tokumitsu, E. *Appl. Phys. Lett.* **2005**, *86*, 162902. (k) Fortunato, E.; Barquinha, P.; Pimentel, A.; Goncalves, A.; Marques, A.; Pereira, L.; Martins, R. *Adv. Mater.* **2005**, *17*, 590. (l) Hoffman, R. L.; Norris, B. J.; Wager, J. F. *Appl. Phys. Lett.* **2003**, *82*, 733.

(4) Nomura, K.; Ohta, H.; Ueda, K.; Kamiya, T.; Hirano, M.; Hosono, H. *Science* **2003**, *300*, 1269.

(5) Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. *Nature* **2004**, *432*, 488.

10.1021/ja100615r
© 2010 American Chemical Society

with low-cost rigid or flexible substrates, especially polymeric substrates. Furthermore, for real-world applications, processes yielding polycrystalline films have traditionally been the only efficient methodologies for large-area depositions. Nevertheless, the mechanical stability, film smoothness, and device uniformity possible for polycrystalline thin-film materials is frequently less than desired for high-performance electronics. In contrast, recent results suggest that the corresponding *amorphous* semiconducting oxide thin films offer many intriguing and potentially useful properties.[5] Thus, amorphous thin-film materials provide superior mechanical flexibility, surface smoothness, and compositional uniformity versus the corresponding crystalline materials due to the lack of grain boundaries.[5] Indeed, amorphous semiconducting In−Ga−Zn−O (a-IGZO)-based devices have recently been fabricated at room temperature on polyethylene terephthalate (PET) by PLD and exhibit moderately high TFT mobilities (∼10 cm^2 V^{-1} s^{-1}).[5]

Although these early results were promising, further understanding of these systems could lead to marked improvements in materials-processing characteristics and carrier mobility, which would enable more efficient large-area film growth, high-throughput fabrication on inexpensive substrates, and advanced high-frequency applications such as S- and X-band radar.[1] In the case of the aforementioned conventional a-Si:H electronics, the Fermi level can barely be displaced into the conduction band mobility edge due to the dense tailing of states arising from structural imperfections such as distorted bond angles between Si atoms and dangling bonds. In contrast, the highly dispersed s-orbital-based conduction bands in post-transition metal oxides have far lower densities of tailing states, and these can be further suppressed by several approaches, such as incorporating structure-relaxing ions and thermal annealing.[7] Therefore, the reported a-IGZO TFT mobility of ∼10 cm^2 V^{-1} s^{-1} is not likely to be the maximum possible value, and further increases are probable, perhaps as high as that of the corresponding crystalline material (∼80 cm^2 V^{-1} s^{-1}).[8] The relatively low TFT mobility versus the corresponding single-crystal device[4] is likely at least partially due to the amorphous microstructure and the annealing temperature, which leaves defects and trap states in the device channel layer. Indeed, optimized annealing temperatures and an improved gate dielectric layer, along with proper device structures, afford higher mobilities, reported to be ∼60 cm^2 V^{-1} s^{-1} for a-IGZO deposited by rf magneton sputtering.[9] Higher In-content channel layers in amorphous $In_9ZnO_{14.5}$ FET devices, also grown by sputtering, are reported to exhibit electron mobilities as high as 108 cm^2 V^{-1} s^{-1}.[10]

Conventional low-pressure metal oxide film growth techniques, such as chemical vapor deposition, sputtering, PLD, molecular beam expitaxy, etc., are widely used for metal oxide film growth due to facile laboratory-scale control of deposition parameters and compositional reproducibility.[11] However, these growth techniques are capital-intensive, can be limited in achievable film area and throughput, and optimized process development for each individual oxide composition can be inefficient and time-consuming.[11,12] In contrast, solution processes such as spin-coating and printing are promising because of the simple, inexpensive equipment, easy control of the deposition parameters, accurate compositional control of the resulting films, and compatibility with large-area high-throughput depositions. Recently, several research groups have reported promising results for TFTs based on solution-processed crystalline ZnO, amorphous Zn−Sn−O, amorphous In−Ga−O, amorphous In−Zn−O, and amorphous In−Ga−Zn−O films.[13] However, typical reported electron mobilities are no greater than ∼10 cm^2 V^{-1} s^{-1}, and then only when the semiconductor films are annealed at very high temperatures (>600 °C).

In this contribution, we report the solution-phase film growth of amorphous ZITO-based TFTs and the dependence of their performance on the semiconductor compositions, $Zn_{9-2x}In_xSn_xO_{9+1.5x}$ ($x = 1-4$) and $ZnIn_{8-x}Sn_xO_{13+0.5x}$ ($x = 1-7$). The optimized amorphous ZITO ($ZnIn_4Sn_4O_{15}$)-based TFTs exhibit electron mobilities exceeding 10 or 100 cm^2 V^{-1} s^{-1}, depending on the gate dielectric, and with current on/off ratios >10^5 for films annealed at relatively low temperatures (400 °C) (Figure 1). We report a detailed compositional, processing, microstructure, and electronic properties investigation aimed at defining those variables which optimize amorphous oxide film mobility and TFT performance.

2. Experimental Section

Precursor Solution Preparation. All reagents were purchased from Sigma-Aldrich Chemicals and were used without further purification. Zinc acetate dihydrate (98%), indium chloride (98%), and tin chloride pentahydrate (99.9%) in various Zn^{2+}:In^{3+}:Sn^{4+}

(6) (a) Lin, W.; Chen, D.; Zhang, J.; Lin, Z.; Huang, J.; Li, W.; Wang, Y.; Huang, F. *Cryst. Growth Des.* **2009**, *9*, 4378. (b) Weher, R. L. *J. Appl. Phys.* **1962**, *33*, 2834. (c) Kanai, Y. *Jpn. J. Appl. Phys.* **1984**, *23*, L12. (d) Yan, M.; Lane, M.; Kannewurf, C. R.; Chang, R. P. H. *Appl. Phys. Lett.* **2001**, *78*, 2342. (e) Nozik, A. *J. Phys. Rev. B* **1972**, *6*, 453. (f) Koida, T.; Fujiwara, H.; Kondo, M. *J. Non-Cryst. Solids* **2008**, *354*, 2805. (g) Yoshida, Y.; Warmsingh, C.; Gessert, T. A.; Young, D. L.; Wood, D. M.; Perkins, J. D.; Coutts, T. J. In *Proceedings*; IEEE 4th World Conference on Photovoltaic Energy Conversion, Osaka, Japan, May 11−18, 2003. (h) Meng, Y.; Yang, X.; Chen, H.; Shen, I.; Jiang, Y.; Zhang, Z.; Hua, Z. *J. Vac. Sci. Technol., A* **2002**, *20*, 288. (i) Wang, X.; Iwaki, H.; Ishitani, H.; Yoshikawa, A. *Phys. Status Solidi C* **2004**, *1*, 1022. (j) Koida, T.; Kondo, M. *J. Appl. Phys.* **2006**, *99*, 123703.

(7) (a) Kumomi, H.; Nomura, K.; Kamiya, T.; Hosono, H. *Thin Solid Films* **2008**, *516*, 1516. (b) Chiang, H. Q.; Hong, D.; Hung, C. M.; Presley, R. E.; Wager, J. F.; Park, C.-H.; Keszler, D. A.; Herman, G. S. *J. Vac. Sci. Technol., B* **2006**, *24*, 2702. (c) Hoffman, R. L. *Solid-State Electron.* **2006**, *50*, 784. (d) Presley, R. E.; Munsee, C. L.; Park, C.-H.; Hong, D.; Wager, J. F.; Keszler, D. A. *J. Phys. D: Appl. Phys.* **2004**, *7*, 2810.

(8) (a) Robertson, J. *Thin Solid Films* **2008**, *516*, 1419. (b) Mort, J.; Knights, J. *Nature* **1981**, *290*, 659.

(9) Joo, M.; Choi, J.; Noh, S.; Park, K.; Ihm, K.; Kim, K.; Kang, T. *Mater. Res. Soc. Symp. Proc.* **2009**, *1108*, A09–08.

(10) Fortunato, E.; Barquinsha, P.; Pimental, A.; Pereira, L.; Goncalves, G.; Martins, R. *Phys. Status Solidi (RRL)* **2007**, *1*, R34.

(11) (a) Choy, K. L. *Prog. Mater. Sci.* **2003**, *48*, 57. (b) Kelly, P. J.; Arnell, R. D. *Vacuum* **2000**, *56*, 159. (c) Willmott, P. R.; Huber, J. R. *Rev. Mod. Phys.* **2000**, *72*, 315. (d) Joyce, B. A. *Rep. Prog. Phys.* **1985**, *48*, 1637.

(12) (a) Park, J.-S.; Kim, K.; Park, Y.-G.; Mo, Y.-G.; Kim, H. D.; Jeong, J. K. *Adv. Mater.* **2009**, *21*, 329. (b) Kim, H. S.; Kim, M.-G.; Ha, Y.-G.; Kanatzidis, M. G.; Marks, T. J.; Facchetti, A. *J. Am. Chem. Soc.* **2009**, *131*, 10826. (c) Park, J.-S.; Song, J.-I.; Heo, Y.-W.; Lee, J.-H.; Kim, J.-J.; Lim, W. T.; Stafford, L.; Norton, D. P.; Pearton, S. J. *J. Vac. Sci. Technol., B* **2006**, *24*, 2737. (d) Im, J.; Auciello, O.; Baumann, P. K.; Streiffer, S. K.; Kaufman, D. Y.; Krauss, A. R. *Appl. Phys. Lett.* **2000**, *76*, 625.

(13) (a) Jeong, S.; Ha, Y.-G.; Moon, J.; Facchetti, A.; Marks, T. J. *Adv. Mater.* **2009**, *21*, 1. (b) Seo, S.-J.; Choi, C. G.; Hwang, Y. H.; Bae, B.-S. *J. Phys. D: Appl. Phys.* **2009**, *42*, 035106. (c) Choi, C. G.; Seo, S.-J.; Bae, B.-S. *Electrochem. Solid-State Lett.* **2008**, *11*, H7. (d) Mensinger, Z. L.; Gatlin, J. T.; Meyers, S. T.; Zakharov, L. N.; Keszler, D. A.; Johnson, D. W. *Angew. Chem., Int. Ed.* **2008**, *47*, 9484. (e) Jeong, S.; Jeong, Y.; Moon, J. *J. Phys. Chem. C* **2008**, *112*, 11082. (f) Ong, B. S.; Li, C.; Li, Y.; Wu, Y.; Loutfy, R. *J. Am. Chem. Soc.* **2007**, *129*, 2750. (g) Chenga, H.-C.; Chen, C.-F.; Tsay, C.-Y. *Appl. Phys. Lett.* **2007**, *90*, 012113. (h) Lee, D.-H.; Chang, Y.-J.; Herman, G. S.; Chang, C.-H. *Adv. Mater.* **2007**, *19*, 843.

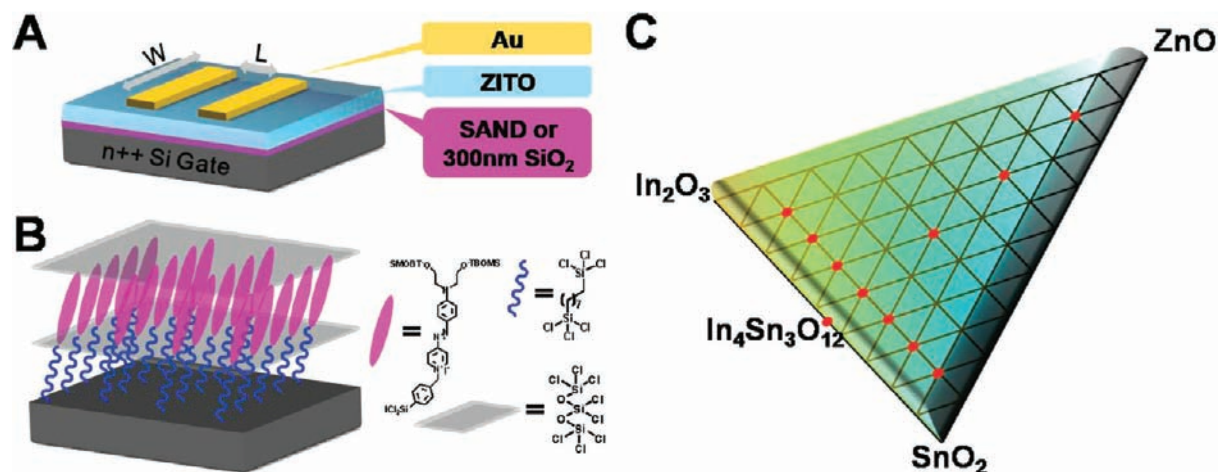

Figure 1. (A) Schematic representation of the TFT structure employed in this study. (B) Structure of an ~5.5 nm thick self-assembled nanodielectric (SAND) gate insulator composed of alkyl (bottom), siloxane (lower middle and top), and stilbazolium (upper middle) layers. This 5.5 nm SAND layer is deposited in three successive iterations to yield a 16.5 nm SAND trilayer. (C) $ZnO-In_2O_3-SnO_2$ ternary phase diagram, where the red dots represent the compositions investigated in this study.

molar ratios were dissolved in 2-methoxyethanol (99%). The overall metal cation concentration was 0.075 and 0.30 M for 10 nm and 30 nm thick films, respectively. Next, ethanolamine (99%) as a stabilizing agent was added to 20 mL vials containing 5 mL of the mixed metal salt solutions, maintaining the ethanolamine:total metal concentration in a 1:1 molar ratio. These clear solutions were then stirred for 2 h with a magnetic stirring bar at room temperature before spin-coating.

Film Deposition. Thermally grown 300 nm SiO_2/p-type silicon wafers and low-resistivity n-type silicon wafers were purchased from Montco Silicon Technologies, Inc. Silicon wafers (1.0 cm × 2.5 cm) with a thermally grown 300 nm SiO_2 layer were cleaned by sonication in pure ethanol, dried under an N_2 flow, and then treated with an O_2 plasma for 5 min. Low-resistivity single-crystal n-type wafers were coated with self-assembled nanodielectric (SAND) as described elsewhere,[14] and were dried under the N_2 flow. Metal salt precursor solutions with varying metal compositions were then spin-coated onto these substrates at a speed of 3500 rpm with acceleration of 3350 rpm/s. Subsequently, the spin-coated films were annealed on a hot plate under air at 250−400 °C for 10 min. The deposition process was then repeated two or three times until the desired film thickness was obtained. The resulting semiconductor film thicknesses were ~10−30 nm, depending on the processing conditions and number of successive metal oxide depositions.

Film Characterization. Surface morphologies of films were imaged with a Digital Instruments Nanoscope III AFM. Grazing incident angle X-ray diffraction (GIAXRD) scans were measured with a Rigaku ATX-G Thin-Film Diffraction Workstation using Cu Kα radiation coupled to a multilayer mirror. Optical spectra were acquired with a Cary 5000 ultraviolet−visible−near-infrared spectrophotometer and were referenced to the spectrum of uncoated Corning 1737F glass. XPS spectra were recorded on Omicron ESCA Probe system with a base pressure of 8×10^{-10} mbar (UHV), using a monochromated Al Kα X-ray source at $h\nu = 1486$ eV. Transmission electron microscopy (TEM) images and selected area electron diffraction (SAED) patterns were obtained using a JEOL JEM-2100F FAST TEM.

TFT Fabrication and Characterization. A top-contact electrode architecture was used for evaluating the present TFT devices. Au source and drain electrodes of 50 nm thickness were deposited by thermal evaporation (pressure $\sim 10^{-6}$ Torr) through shadow masks, affording channel dimensions of 100 μm (*L*) × 1000 μm (*W*) with appropriate precautions for TFT measurement accuracy.[15] TFT device characterization was performed on a customized probe station in dry air with a Keithley 6430 subfemtometer and a Keithley 2400 source meter, operated by a locally written Labview program and GPIB communication. The top-contact Si/SiO_2/metal oxide/Au, Si/SAND/metal oxide/Au device structures are shown in Figure 1A. SAND film growth procedures were carried out as described previously.[14]

TFT and Capacitor Devices Fabricated with Patterned-$ZnIn_4Sn_4O_{15}$ Films. For patterned TFT fabrication, a Au protecting layer defining the patterned region was deposited on Si/SAND/ZITO substrates by thermal evaporation using a shadow mask (5.5 mm × 10 mm). The areas not coated with the Au were etched with a CH_4/H_2 plasma at a flow rate of 5/25 sccm CH_4/H_2 (pressure = 11 mTorr, rf power = 100 W).[16] After etching, the Au protecting layer was removed by sonication in ethanol. The TFT structure was then completed by Au source and drain electrode deposition [(100 μm (*L*) × 5000 μm (*W*)] as for the unpatterned devices.

For Si/SAND/ZITO/Au capacitor fabrication, Au pads (100 μm × 100 μm) were deposited on Si/SAND/ZITO substrates by thermal evaporation using a shadow mask. The Au-uncoated areas were then etched by a CH_4/H_2 plasma at a flow rate of 5/25 sccm CH_4/H_2 (pressure = 11 mTorr, rf power = 100 W), and these devices were used directly for capacitance and leakage current measurements.

3. Results

In this section, we first discuss the solution-phase film deposition process and then analyze the ZITO film microstructural and morphological properties as a function of the film metal composition and growth parameters. Next, bottom gate/top contact structure thin-film transistors are fabricated with the a-ZITO semiconducting films. The device performance dependence on film stoichiometry, microstructure, and the semiconductor-gate dielectric interface is finally characterized as a function of metal composition and gate dielectric material, respectively.

3.1. ZITO Film Synthesis. In typical oxide sol−gel-based solution film growth processes, 2-methoxyethanol is commonly used as the solvent since it can act as a bridging ligand and

(14) (a) DiBenedetto, S. A.; Facchetti, A.; Ratner, M. A.; Marks, T. J. *Adv. Mater.* **2009**, *21*, 1407. (b) Yoon, M. H.; Facchetti, A.; Marks, T. J. *Proc. Natl. Acad. Sci. U.S.A.* **2005**, *102*, 4678. (c) Yoon, M.-H.; Yan, H.; Facchetti, A.; Marks, T. J. *J. Am. Chem. Soc.* **2005**, *127*, 10388.
(15) Okamura, K.; Nikolova, D.; Mechau, N.; Hahn, H. *Appl. Phys. Lett.* **2009**, *94*, 183503.

(16) Price, S. P.; Henzie, J.; Odom, T. W. *Small* **2007**, *3*, 372.

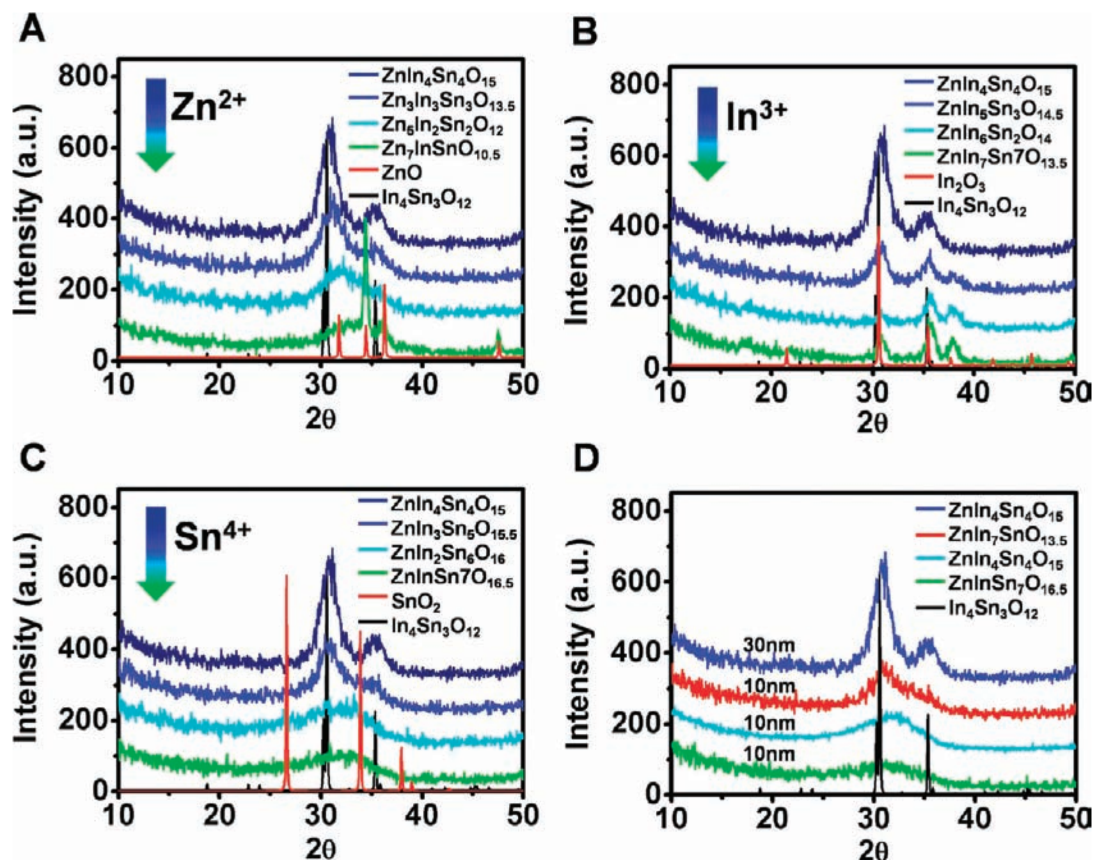

Figure 2. Grazing incident angle X-ray diffraction (GIAXRD) patterns of ZITO films on n++Si wafers having the indicated compositions: (A) $Zn_{9-2x}In_xSn_xO_{9+1.5x}$ ($x = 1-4$) (B) $ZnIn_{8-x}Sn_xO_{13+0.5x}$ ($x = 1-4$) (C) $ZnIn_{8-x}Sn_xO_{13+0.5x}$ ($x = 4-7$). All films for A−C are 30 nm thick. (D) $ZnIn_{8-x}Sn_xO_{13+0.5x}$. All films are 10 nm thick except that corresponding to the blue line (30 nm thick).

thus stabilize intermediate high-molecular weight oligomers.[17] Also, 2-methoxyethanol has a low viscosity and good solubility for the various metal precursors.[17] In the present study, 2-methoxyethanol was used as the solvent and ethanolamine as a stabilizing agent and solubility enhancer. To determine optimum spin-coating procedures and annealing temperatures, film microstructure and TFT device performance were systematically investigated as a function of film processing conditions (see more about these techniques below), and possible decomposition products were assayed by XPS for annealing temperatures in the range 250−400 °C.

3.2. ZITO Film Characterization. The morphology and microstructure of the present ZITO films grown on two different dielectric surfaces were investigated by grazing incident angle X-ray diffraction (GIAXRD), transmission electron microscopy (TEM), atomic force microscopy (AFM), and X-ray photoelectron spectroscopy (XPS). Figure 2 shows GIAXRD scans of ZITO films having different metal compositions. These data show that at high Zn and In contents, the ZnO (Figure 2A) and In_2O_3 (Figure 2B) phases, respectively, are clearly present. Correspondingly, when the Zn^{2+} concentration is low, In_2O_3 or $In_4Sn_3O_{12}$ reflections are observed. Interesting, for fixed In^{3+} and Sn^{4+} ratios, increasing the Zn^{2+} concentration results first in amorphous films and eventually in a mixture of ZnO and amorphous phase materials. Furthermore, with increasing Zn^{2+} content, the amorphous phase diffuse scattering maximum shifts toward higher angles, reflecting a contraction in the average metal−oxygen distance.

The pronounced tendency for a composition region of amorphous film formation corresponds to the multiple phase coexistence region in the $ZnO-In_2O_3-SnO_2$ phase diagram, which is based on high temperature bulk synthesis data at 1275 °C.[18] Substituting impurities in the corresponding phase can inhibit the crystalline growth by blocking self-diffusion in the crystallites, or the impurities in the amorphous matrix can impede diffusion processes required for crystallite growth.[19] Furthermore, atomically mixed metal precursors derived from solution may be difficult to crystallize in the multiple-phase region since each phase could in principle retard the growth of the other crystalline phases.[19] Interestingly, in diffraction scans, we observe the Bragg reflections of crystalline $In_4Sn_3O_{12}$ for Zn:In:Sn = 1:4:4 at $2\theta = 30.6°$ and 35.4°. We also observe the highest field effect mobility at the $ZnIn_4Sn_4O_{15}$ composition (see Tables 1 and 2). Since the bixbyite In_2O_3 and $In_4Sn_3O_{12}$ structures exhibit very similar XRD patterns, it is difficult to unambiguously assign diffraction data from the 30 nm $ZnIn_4Sn_4O_{15}$ films to the $In_4Sn_3O_{12}$ phase solely on the basis of the GIAXRD data in Figure 2. However, considering the chemical composition of $ZnIn_4Sn_4O_{15}$ films and a previous analysis of Sn doping in rhombohedral In_2O_3 films which leads to structural densification due to the small Sn^{4+} size,[20] it is

(17) (a) Yoon, K. H.; Park, J. H.; Kang, D. H. *J. Am. Ceram. Soc.* **1995**, *78*, 2267. (b) Livage, C.; Safari, A.; Klein, L. C. *J. Sol-Gel Sci. Technol.* **1994**, *2*, 605.

(18) Harvey, S. P.; Popplemeier, K. R.; Mason, T. *J. Am. Ceram. Soc.* **2008**, *91*, 3683.

(19) (a) Song, P. K.; Akao, H.; Kamei, M.; Shigesato, Y.; Yasui, I. *Jpn. J. Appl. Phys.* **1999**, *38*, 5224. (b) Kim, K. S.; Turnbull, D. *J. Appl. Phys.* **1974**, *45*, 3447.

(20) Nadaud, N.; Lequeux, N.; Nanot, M.; Jové, J.; Roisnel, T. *J. Solid State Chem.* **1998**, *135*, 140.

Table 1. Amorphous Zinc Indium Tin Oxide Semiconductor-Based TFT Performance Data for Devices Having 300 nm Thick SiO_2 as the Gate Dielectric, for Semiconducting Films Spin-Coated from Formulations Having the Indicated Metal Atomic Ratios

ZITO composition	μ^{sat} ($cm^2 V^{-1} s^{-1}$)	I_{on}/I_{off}	V_{th} (V)	S (V/dec)	D_{it} ($cm^{-2} eV^{-1}$)[a]
$ZnInSn_7O_{16.5}$	1.4 ± 0.1	10^5-10^6	63.7	11.1	1.3×10^{13}
$ZnIn_2Sn_6O_{16}$	1.7 ± 0.2	10^4-10^5	32.3	11.2	1.3×10^{13}
$ZnIn_3Sn_5O_{15.5}$	6.6 ± 0.2	10^4-10^5	42.3	10.7	1.2×10^{13}
$ZnIn_4Sn_4O_{15}$	11.4 ± 0.8	10^4-10^5	41.3	9.5	1.1×10^{13}
$ZnIn_5Sn_3O_{14.5}$	9.1 ± 0.5	10^3	22.4	14.9	1.7×10^{13}
$ZnIn_6Sn_2O_{14}$	4.4 ± 0.5	10^2	27.4	29.9	3.5×10^{13}
$ZnIn_7SnO_{13.5}$	–	–	–	–	

ZITO composition	μ^{sat} ($cm^2 V^{-1} s^{-1}$)	I_{on}/I_{off}	V_{th} (V)	S (V/dec)	D_{it} ($cm^{-2} eV^{-1}$)[a]
$ZnIn_4Sn_4O_{15}$	11.4 ± 0.8	10^4-10^5	41.3	9.5	1.1×10^{13}
$Zn_3In_3Sn_3O_{13.5}$	1.7 ± 0.1	10^6-10^7	39.7	6.2	7.1×10^{12}
$Zn_5In_2Sn_2O_{12}$	1.8 ± 0.2	10^6	78.8	6.2	7.1×10^{12}
$Zn_7InSnO_{10.5}$	0.06 ± 0.03	10^4	79.9	4.0	4.6×10^{12}

[a] D_{it}: interface state density.

Table 2. Amorphous Zinc Indium Tin Oxide Semiconductor-Based TFT Performance Data for Devices Having SAND (16.5 nm thick) as the Gate Dielectric, for Semiconducting Films Spin-Coated from Formulations Having the Indicated Metal Atomic Ratios

ZITO composition	μ^{sat} ($cm^2 V^{-1} s^{-1}$)	I_{on}/I_{off}	V_{th} (V)	S (V/dec)	D_{it} ($cm^{-2} eV^{-1}$)[a]
$ZnInSn_7O_{16.5}$	9 ± 5	10^3	1.8	0.28	6.5×10^{12}
$ZnIn_3Sn_5O_{15.5}$	87 ± 11	10^5-10^6	1.2	0.31	7.4×10^{12}
$ZnIn_4Sn_4O_{15}$	100 ± 13	10^5-10^6	1.0	0.23	5.0×10^{12}
patterned $ZnIn_4Sn_4O_{15}$	90 ± 10	10^4-10^5	1.0	0.2	5.0×10^{12}
$ZnIn_5Sn_3O_{14.5}$	65 ± 15	10^4-10^5	1.3	0.50	1.3×10^{13}
$ZnIn_6Sn_2O_{14}$	28 ± 10	10^2	0.8	0.70	1.9×10^{13}

ZITO composition	μ^{sat} ($cm^2 V^{-1} s^{-1}$)	I_{on}/I_{off}	V_{th} (V)	S (V/dec)	D_{it} ($cm^{-2} eV^{-1}$)[a]
$ZnIn_4Sn_4O_{15}$	100 ± 13	10^5-10^6	1.0	0.23	5.0×10^{12}
$Zn_3In_3Sn_3O_{13.5}$	27 ± 4	10^6-10^7	1.5	0.09	9.1×10^{11}

[a] D_{it}: interface state density.

reasonable to assign the GIAXRD data for the present $ZnIn_4Sn_4O_{15}$ films to the dense $In_4Sn_3O_{12}$ crystal structure.

The $In_4Sn_3O_{12}$ phase has been synthesized at high temperatures (>1300 °C) for bulk samples, however crystalline $In_4Sn_3O_{12}$ films have only been grown at 350 °C by dc magnetron sputtering.[18,21] Figure 2D shows that the 10 nm thick films corresponding to $ZnIn_4Sn_4O_{15}$ compositions are amorphous. This behavior is significantly different from that of the corresponding 30 nm thick $ZnIn_4Sn_4O_{15}$ films which are crystalline at these compositions. It is known that in general, thin films more readily form amorphous phases, since in cases where the film–substrate interactions stabilize the amorphous phase, the increased interface-to-volume ratio enhances the amorphous phase stabilization and increases the crystallization temperature.[22] The amorphous nature of the 10 nm $ZnIn_4Sn_4O_{15}$ films is further confirmed by TEM. Panels A and B of Figure 3 show selected area electron diffraction patterns for 10 and 30 nm thick $ZnIn_4Sn_4O_{15}$ films, respectively. These data demonstrate that the former films are amorphous, whereas the latter are nanocrystalline, in agreement with the GIAXRD data. C and D of Figures 3 also show tapping-mode AFM images of 10 nm thick $ZnIn_4Sn_4O_{15}$ films on Si/SiO_2 and Si/SAND substrates, respectively. These films exhibit rms roughness of <0.2 nm and ~3 nm, respectively, with the latter reflecting the slightly rougher SAND topography.[12b] In Figure 4, optimized $ZnIn_4Sn_4O_{15}$ composition films grown on the Corning 1737F glass substrates are shown to have very good optical transparency in the visible regime by transmission optical spectroscopy.

Figure 5 shows XPS spectra of 10 nm $ZnIn_4Sn_4O_{15}$ films after 400 °C annealing. From the respective binding energies (Table S1), the metals are in the oxidation states Zn^{2+}, In^{3+}, and Sn^{4+}.[23] More importantly, the broad peak around 531 eV corresponding to the O 1s core level, can be deconvoluted into three features, located at 529.9, 531.2, and 531.9 eV. The 529.9 eV peak is assigned to lattice oxygen and the 531.2 eV peak to lattice oxygen in oxygen-deficient regions.[23c] The metal hydroxide and/or oxy-hydroxide oxygen feature is observed at a binding energy near 531.9 eV.[23a,c]

Conversion of the metal precursors into metal oxide films was studied by XPS for 10 nm $ZnIn_4Sn_4O_{15}$ films. For each annealing temperature, detailed scans for C 1s and O 1s core levels were analyzed (Figure 6 below). Pronounced changes in the peak shapes and deconvoluted peak positions are observed after 300 °C annealing. The three deconvoluted O 1s core level ionization features observed can be assigned to a metal oxide lattice peak, metal oxide lattice peak in the oxygen-deficient region, and a metal hydroxide peak. The same assignments are made in the 400 °C annealed film (Figure 6). For C 1s core level ionizations, the 284.5 eV feature is attributed to C–C and C–H moieties, and is usually used as reference peak.[23c] The higher binding energy peaks at 285.7 and 288.6 eV can be assigned to carbon oxide groups.[23b] These three deconvoluted C1s peaks (284.5, 285.7, and 288.6 eV) are attributed to adventitious surface contamination arising from (CH_x)-like carbon and carbon oxides.[23c,b] For the 250 °C-annealed film, the complicated and unassigned peaks are denoted with black arrows. Considering the starting precursors, ethanolamine and zinc acetate, the 287 and 289.5 eV peaks are tentatively assigned to O–C, N–C=O, or O–C=O residues from the organic matrix. Those assignments are in agreement with the observed O1s core level peaks. The 532.5 and 531.1 eV ionizations are also tentatively attributed to C–O and C=O moieties.[23b]

3.3. ZITO Thin-Film Transistor Fabrication and Characterization. Figure 1A shows the bottom-gate top-contact TFT structure employed in this study. The present ZITO-based TFTs were fabricated on doped Si substrates coated with a 300 nm thick SiO_2 layer ($C_i \approx 11$ nF/cm^2) or a 16.5 nm self-assembled nanodielectric (SAND) multilayer ($C_i \approx 280$ nF/cm^2)[14] functioning as gate dielectric materials. ZITO films with incrementally varied metal compositions were deposited by spin-coating (see Experimental Section for details) and subsequently annealed at 400 °C under air. The TFT structures were completed by thermal evaporation of Au source-drain contacts through a shadow mask. All ZITO TFT measurements were performed in ambient air, and the $I_{SD}-V_G$ curves were analyzed using the standard metal-oxide-semiconductor field-effect transistor (MOS-

(21) (a) González, G. B.; Mason, T. O.; Quintana, J. P.; Warschkow, O.; Ellis, D. E.; Hwang, J.-H.; Hodges, J. P.; Jorgensen, J. D. *J. Appl. Phys.* **2004**, *96*, 3912. (b) Minami, T.; Takeda, Y.; Takata, S.; Kakumu, T. *Thin Solid Films* **1997**, *308*, 13.

(22) (a) Zacharias, M.; Bläsing, J.; Veit, P.; Tsybeskov, L.; Hirschman, K.; Fauchet, P. M. *Appl. Phys. Lett.* **1999**, *74*, 2614. (b) Muranaka, S. *Jpn. J. Appl. Phys.* **1991**, *30*, L2062. (c) Muranaka, S.; Bando, Y.; Takada, T. *Thin Solid Films* **1987**, *151*, 355.

(23) (a) Biswas, P. K.; De, A.; Dua, L. K.; Chkoda, L. *Bull. Mater. Sci.* **2006**, *29*, 323. (b) Crist, V. B. *Handbooks of Monochromatic XPS Spectra: The Elements and Native Oxides*; XPS International LLC: Mountain View, CA, 2004. (c) Donley, C; Dunphy, D.; Panie, D.; Carter, C.; Nebesny, K.; Lee, P.; Alloway, D.; Armstrong, N. R. *Langmuir* **2002**, *18*, 450. (d) Fan, J. C. C.; Goodenough, J. B. *J. Appl. Phys.* **1977**, *48*, 3524.

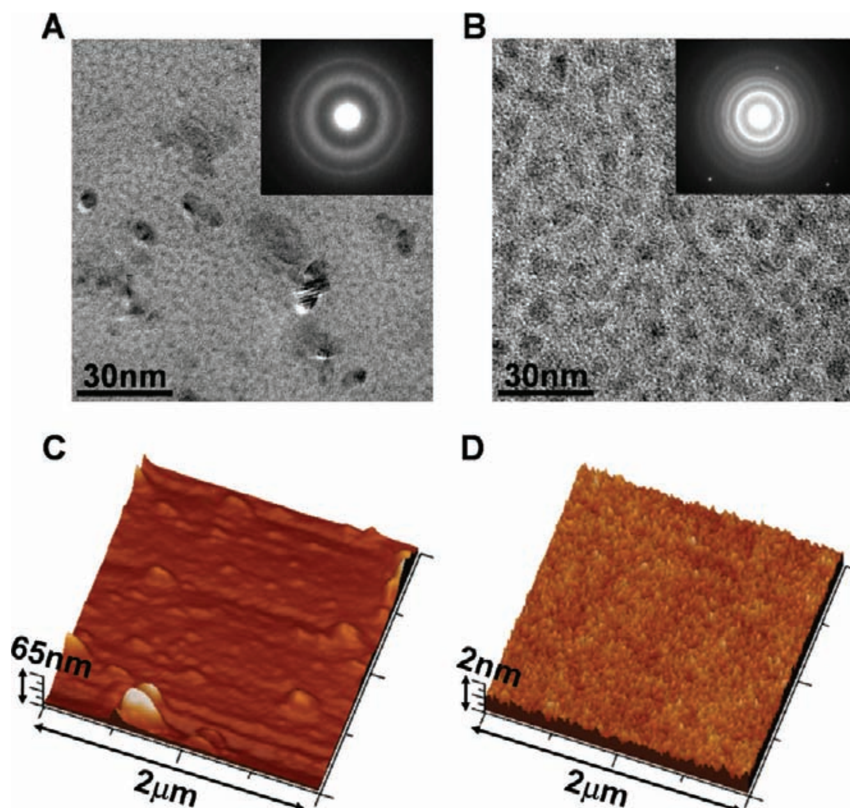

Figure 3. TEM and AFM images of a-$ZnIn_4Sn_4O_{15}$ films: (A) plane view TEM images and their corresponding selected area electron diffraction pattern (inset) of a 10 nm thick film and (B) a 30 nm thick a-$ZnIn_4Sn_4O_{15}$ film on native oxide/n++Si. AFM images of 10 nm thick a-$ZnIn_4Sn_4O_{15}$ films deposited (C) on 16.5 nm SAND (rms roughness ~3 nm) and (D) on 300 nm thermal SiO_2/p+Si (rms roughness <0.2 nm).

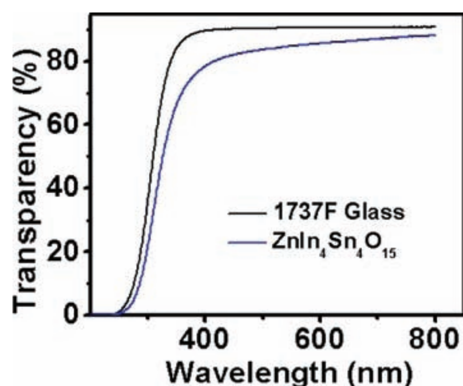

Figure 4. Optical transmission spectrum of a 10 nm a-$ZnIn_4Sn_4O_{15}$ film on Corning 1737F glass.

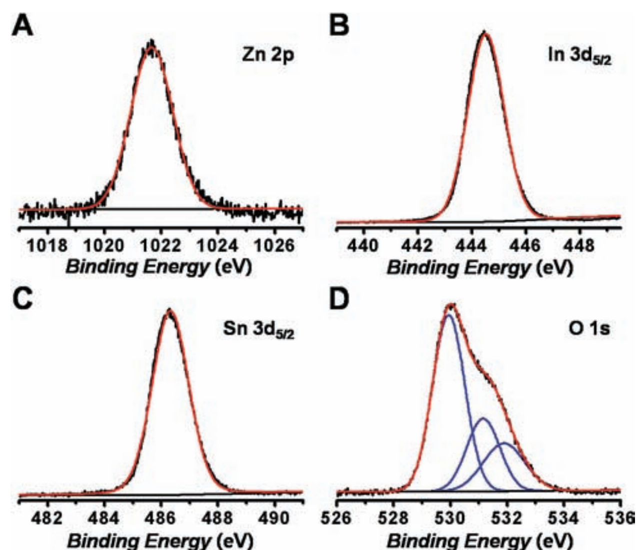

Figure 5. XPS spectra for the, (A) Zn 2p, (B) Sn $3d_{5/2}$, (C) In $3d_{5/2}$, and (D) O 1s signals of a 10 nm a-$ZnIn_4Sn_4O_{15}$ film annealed at 400 °C. The black lines indicate experimental data, while the red and blue lines are the fitted curves.

FET) model.[24,25] For each composition and dielectric batch, at least five devices were measured, and the tabulated results are averages (see below). Figures 7, 8, 9 and 10 collect representative output (I_{DS} vs V_{DS}) and transfer (I_{DS} vs V_G) plots for the TFTs with both SiO_2 and SAND as the gate dielectric. For unpatterned ZITO TFTs, all measurements were made with 100 μm channel length and 1000 μm channel width contacts, taking appropriate precautions to ensure accurate device parameters.[15] For patterned ZITO TFTs, the

(24) (a) Greve, D. W. *Field Effect Devices and Application: Devices for Portable, Low-power, and Imaging Systems*; Prentice-Hall: New Jersey, 1988. (b) Sze, S. M. *Physics of Semiconductor Devices*; John Wiley & Sons: New York, 1981.

(25) (a) Liu, J.; Buchholz, D. B.; Chang, R. P. H.; Facchetti, A.; Marks, T. J. *Adv. Mater.* **2010**, *22*, 2333. (b) Chen, P.-C.; Shen, G.; Chen, H.; Ha, Y.-G.; Wu, C.; Sukcharoenchoke, S.; Fu, Y.; Liu, J.; Facchetti, A.; Marks, T. J.; Thompson, M. C.; Zhou, C. *ACS Nano* **2009**, *3*, 3383. (c) Kim, H. S.; Facchetti, A.; Marks, T. J. *J. Am. Chem. Soc.* **2008**, *130*, 12580. (d) Byrne, P. D.; Facchetti, A.; Marks, T. J. *Adv. Mater.* **2008**, *20*, 2319. (e) Lee, K.; Lu, G.; Facchetti, A.; Janes, D. B.; Marks, T. J. *Appl. Phys. Lett.* **2008**, *92*, 123509. (f) Ju, S.; Ishikawa, F.; Chen, P.; Chang, H.-K.; Zhou, C.; Ha, Y.-G.; Liu, J.; Facchetti, A.; Marks, T. J.; Janes, D. B. *Appl. Phys. Lett.* **2008**, *92*, 222105. (g) Ju, S.; Facchetti, A.; Xuan, Y.; Liu, J.; Ishikawa, F.; Ye, P.; Zhou, C.; Marks, T. J.; Janes, D. B. *Nature Nanotechnol.* **2007**, *2*, 378.

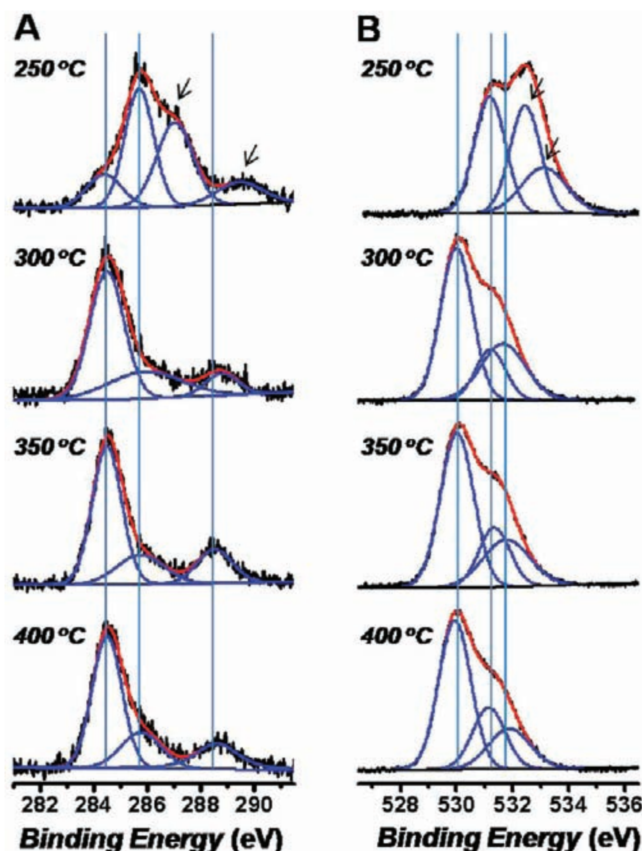

Figure 6. XPS spectra for the: (A) C 1s and (B) O 1s signal regions of a 10 nm a-$ZnIn_4Sn_4O_{15}$ film annealed at the indicated temperatures. The black lines indicate experimental data, while the red and blue lines are fitted curves. The arrows indicate the unassigned peaks discussed in the text.

measurements were made using 100 μm channel length and 5000 μm channel width contacts.

When a number of conditions are satisfied (e.g., $V_{DS} \geq V_G$), the TFT channel becomes pinched, and the source-drain current enters the saturation regime. The carrier mobility (μ) and threshold voltage (V_{th}) can be calculated from the slope and the horizontal intercept of a linear part in $I_{DS,Sat}^{1/2}$ vs V_G plot, respectively, according to eqs 1 and 2; where C_i is the capacitance per unit area of the dielectric layer,

$$\mu^{sat} = \left(\frac{\partial\sqrt{I_{DS}}}{\partial V_G}\right)^2 \frac{2L}{WC_i} \tag{1}$$

$$V_{th,sat} = V_G - \sqrt{\frac{2I_{DS}L}{WC_i\mu}} \tag{2}$$

L and W are the channel length and width, respectively. The interface state densities (D_{it}) of the devices were estimated from the subthreshhold swing values using eq 3, where k is the Boltzmann constant, T the absolute temperature, and q the charge of the carrier. Tables 1, 2, and 3 summarize the extracted TFT performance parameters such as carrier mobility, threshold voltage, subthreshold swing, and current on/off ratio as a function of TFT semiconductor composition and gate dielectric.

$$S = \frac{dV_G}{d(\log I_{SD})} \simeq \ln 10\frac{kT}{q}\left[1 + \frac{qD_{it}}{C_i}\right] \tag{3}$$

3.3.1. Off-Current Dependence on Film Composition and Dielectric Identity. For ZITO films grown on Si/SiO_2 with a 100 V source-drain bias, a TFT 100 μm channel length and a 1000 μm channel width, an increase in the off-current from 10^{-10} to 10^{-6} A is observed on increasing the In content from $ZnInSn_7O_{16.5}$ to $ZnIn_6Sn_2O_{14}$. Further increases in In content up to $ZnIn_7SnO_{13.5}$ are accompanied by a significant off-current increase up to 10^{-4}−10^{-3} A. Increasing the Zn^{2+} content from $ZnIn_4Sn_4O_{15}$ to $Zn_7InSnO_{10.5}$ induces a fall in the off-current from 10^{-8} to 10^{-11} A. Similar trends in off-current behavior are observed on the SAND gate dielectric in Figure 9. With a 2.5 V source-drain bias for a 100 μm channel length and a 1000 μm channel width on SAND, an increase in the off-current from 10^{-10} A to 10^{-6} A is observed by increasing the In content from $ZnInSn_7O_{16.5}$ to $ZnIn_6Sn_2O_{14}$. For SAND-based devices, we observe an additional drop in off-current for the relatively high off-current compositions. For $ZnIn_4Sn_4O_{15}$, 10^{-8} A with 100 V bias on SiO_2 is measured, however 10^{-10} A is obtained with 2.5 V bias on SAND.

3.3.2. Saturation Mobility (μ^{sat}) Dependence on Film Composition and Dielectric Identity. From Figure 11a, the saturation

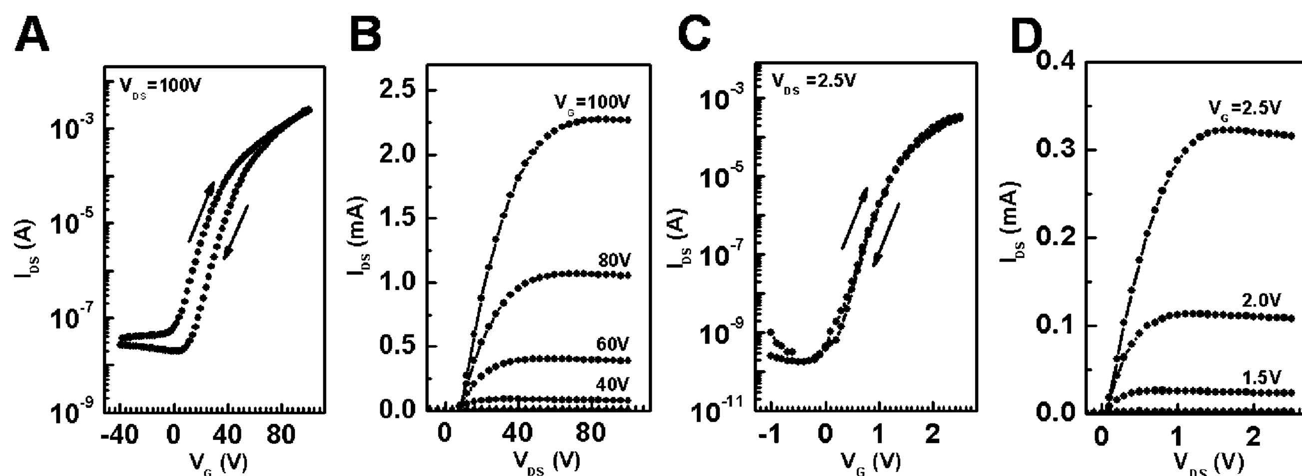

Figure 7. Representative transfer (A, C) and output (B, D) plots for ZITO-based TFTs (a-$ZnIn_4Sn_4O_{15}$, T_a = 400 °C) having the following structures: (A) and (B) Si/SiO_2 (300 nm)/ZITO (10 nm)/Au (50 nm), L = 100 μm, W = 1000 μm. (C) and (D). Si/SAND (16.5 nm)/ZITO (10 nm)/Au (50 nm), L = 100 μm, W = 1000 μm. For each composition and dielectric batch, at least five devices were measured, and tabulated results are averages (see below).

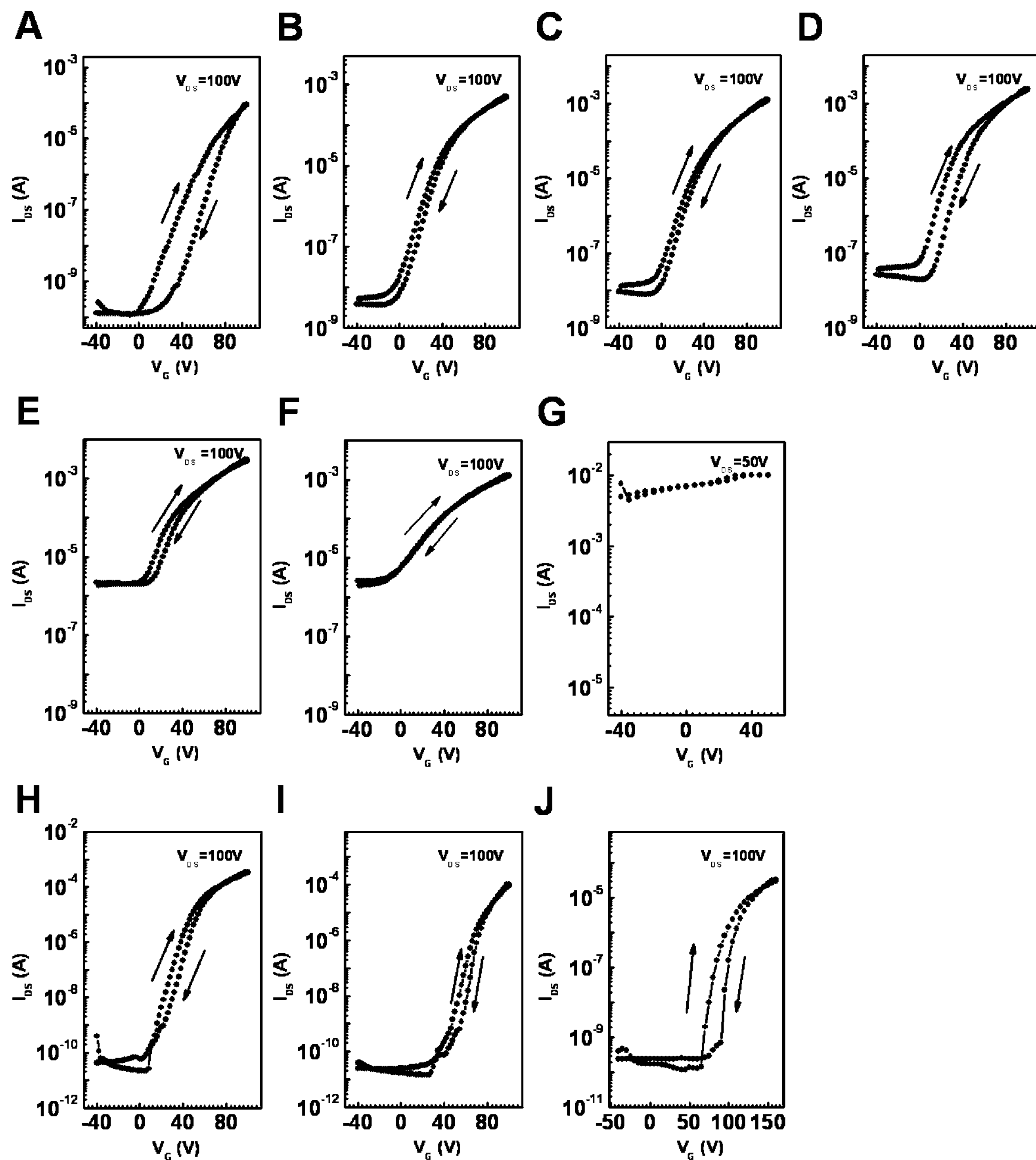

Figure 8. Representative transfer plots for ZITO-based TFTs (Si/SiO_2 (300 nm)/ZITO (10 nm)/Au (50 nm), $L = 100$ μm, $W = 1000$ μm, $T_a = 400$ °C) having the following compositions of: a-$ZnIn_{8-x}Sn_xO_{13+0.5x}$ (A) $x = 7$.(B) $x = 6$. (C) $x = 5$. (D) $x = 4$. (E) $x = 3$. (F) $x = 2$. (G) $x = 1$. $Zn_{9-2x}In_xSn_xO_{9+1.5x}$: (H) $x = 3$. (I) $x = 5$. (J) $x = 7$.

mobility trends reveal a maximum film value for the $ZnIn_4Sn_4O_{15}$ composition at $ZnIn_{8-x}Sn_xO_{13+0.5x}$, $x = 1-7$. Furthermore, we observe a significant increase in mobility for ZITO grown on SAND versus SiO_2. Such an increase in oxide semiconductor mobility with SAND introduction is consistent with several previous reports from this laboratory (see additional Discussion below).[25] Maintaining the In^{3+}:Sn^{4+} ratio at 1:1, while increasing the Zn^{2+} content invariably depresses the mobility for either SAND or SiO_2 as the gate insulator (Figure 11B).

3.3.3. Current On/Off (I_{on}/I_{off}) Ratio Dependence on Semiconductor Film Composition and Dielectric Identity. From the present results, it can be seen that the TFT current on/off ratio is strongly correlated with the film mobility and off-current. For the SiO_2 dielectric-based TFTs with high In and Sn content, we observe a strong dependence of the current on/off ratio on the off-current. The mobility dispersion is only 8x between the maximum observed value, 11.4 cm^2 V^{-1} s^{-1} for $ZnIn_4Sn_4O_{15}$, and the minimum value, 1.4 cm^2 V^{-1} s^{-1} for $ZnInSn_7O_{16.5}$; however, the off-current differs by 10^4x between 10^{-10} A for $ZnInSn_7O_{16.5}$

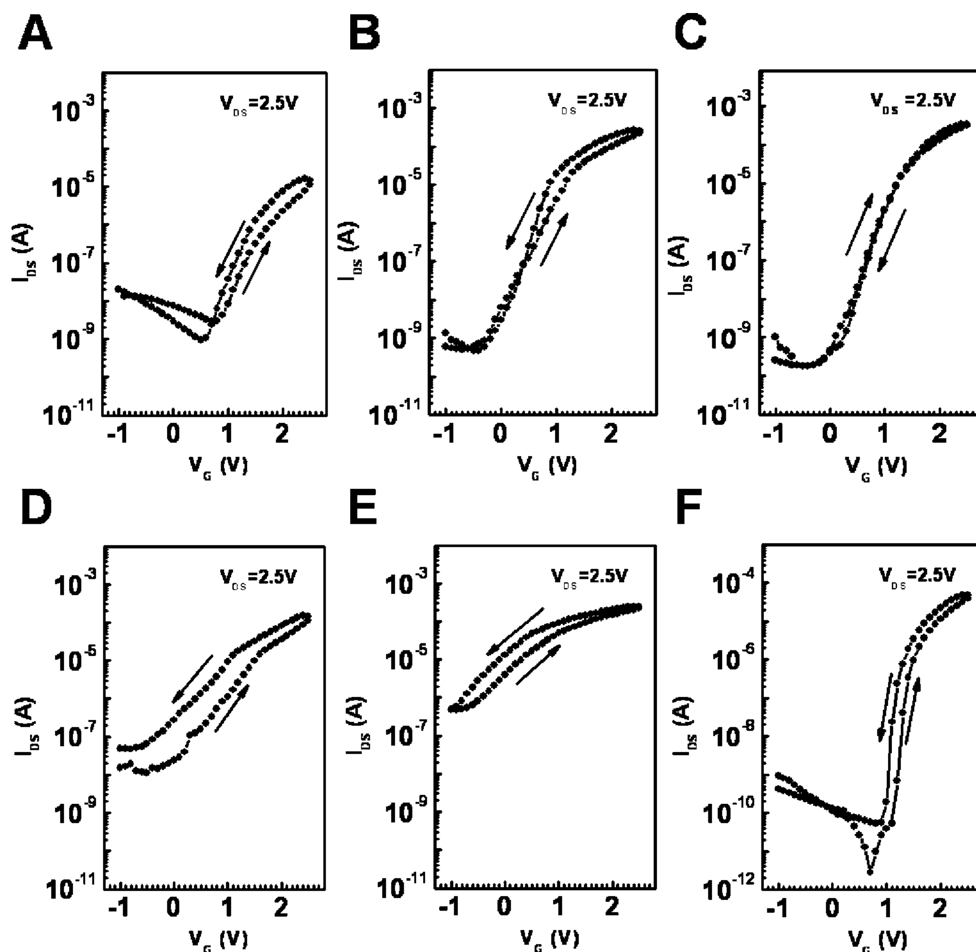

Figure 9. Representative transfer plots for ZITO-based TFTs (Si/SAND (16.5 nm)/ZITO (10 nm)/Au (50 nm), $L = 100$ μm, $W = 1000$ μm., $T_a = 400$ °C) having the following compositions of: a-$ZnIn_{8-x}Sn_xO_{13+0.5x}$ (A) $x = 7$.(B) $x = 5$. (C) $x = 4$. (D) $x = 3$. (E) $x = 1$. (F) $Zn_3In_3Sn_3O_{13.5}$.

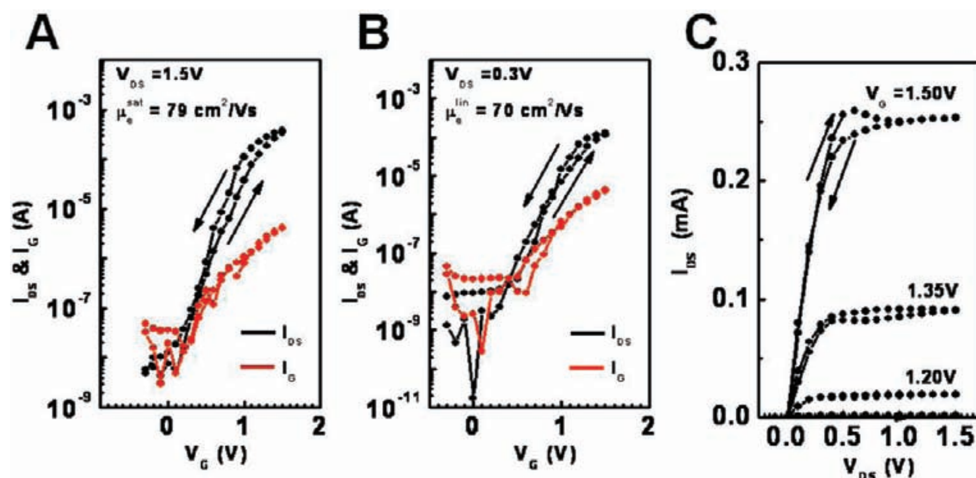

Figure 10. Representative transfer (A, B) and output (C) plots for patterned ZITO-based TFTs (a-$ZnIn_4Sn_4O_{15}$, $T_a = 400$ °C) having. Si/SAND (16.5 nm)/patterned ZITO (10 nm)/Au (50 nm), $L = 100$ μm, $W = 5000$ μm.

and 10^{-6} A for $ZnIn_4Sn_4O_{15}$. Thus, a general trend of increasing current on/off ratio is observed with increasing Sn^{4+} content (Figure 12A). When the gate dielectric is changed to SAND, the TFT current on/off ratio is also maximized at the $ZnIn_4Sn_4O_{15}$ stoichiometry with $I_{on}/I_{off} = 10^5-10^6$. For high In^{3+} content devices ($ZnIn_6Sn_2O_{14}$), the large off-current is principally responsible for the low current modulation efficiency, but for the high Sn^{4+} content sample, the low mobility and high threshold voltage are the principal cause of the low on-current and low I_{on}/I_{off} ratio.

On increasing the Zn^{2+} content, we observe an increased current on/off ratio on proceeding from $ZnIn_4Sn_4O_{15}$ to $Zn_5In_2Sn_2O_{12}$ on a SiO_2 dielectric (Figure 12B). Further increases in the Zn^{2+} content to $Zn_7InSnO_{10.5}$ induce a fall in the current on/off ratio due to a significant mobility decline and an increase in the threshold voltage (Figure 12B). Similar responses are

Table 3. a-$ZnIn_4Sn_4O_{15}$ Semiconductor-Based TFT Performance with 300 nm Thick SiO_2 as the Gate Dielectric for Semiconducting Films Spin-Coated and Annealed at the Indicated Temperatures

temperature (°C)	μ^{sat} (cm^2 V^{-1} s^{-1})	I_{on}/I_{off}	V_{th} (V)	S (V/dec)	D_{it} (cm^{-2} eV^{-1})[a]
250		inactive			
300	10^{-2}	10^5-10^6	66.2	9.8	1.1×10^{13}
350	0.93 ± 0.1	10^5	51.2	8.3	9.6×10^{12}
400	11.4 ± 0.8	10^4-10^5	41.3	9.5	1.1×10^{13}

[a] D_{it}: interface state density.

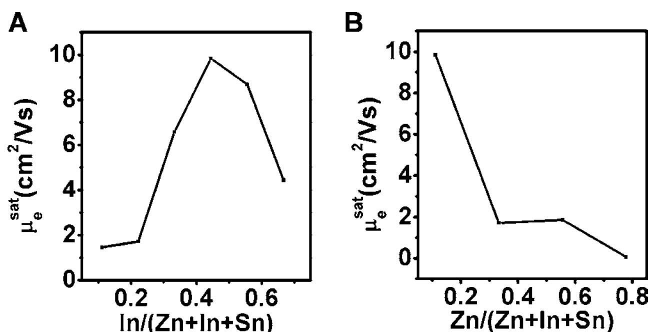

Figure 11. (A) Saturation mobility (μ^{sat}) plots as a function of $[In^{3+}]/[Zn^{2+}+In^{3+}+Sn^{4+}]$ ratio for $ZnIn_{8-x}Sn_xO_{13+0.5x}$ films on SiO_2/Si. (B) Saturation mobility (μ^{sat}) plots as a function of $[Zn^{2+}]/[Zn^{2+}+In^{3+}+Sn^{4+}]$ ratio for $Zn_{9-2x}In_xSn_xO_{9+1.5x}$ films on Si/SiO_2.

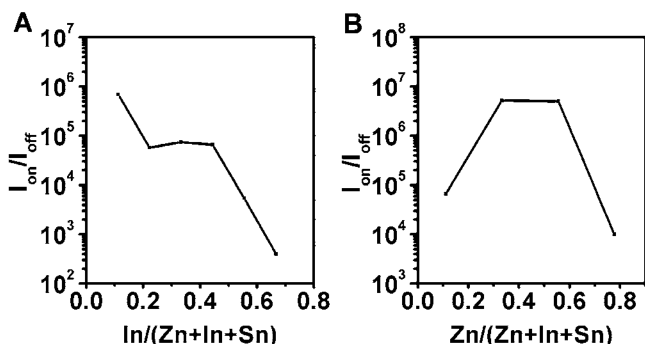

Figure 12. (A) I_{on}/I_{off} plots as a function of $[In^{3+}]/[Zn^{2+}+In^{3+}+Sn^{4+}]$ ratio for a-$ZnIn_{8-x}Sn_xO_{13+0.5x}$ films on SiO_2/Si. (B) I_{on}/I_{off} plots as a function of $[Zn^{2+}]/[Zn^{2+}+In^{3+}+Sn^{4+}]$ ratio for a-$Zn_{9-2x}In_xSn_xO_{9+1.5x}$ films on Si/SiO_2.

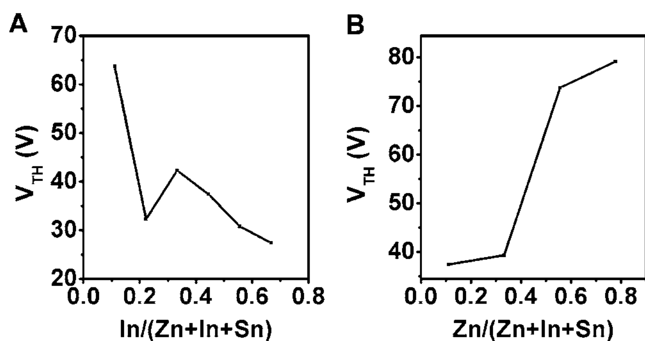

Figure 13. (A) Threshold voltage (V_{th}) plots as a function of $[In^{3+}]/[Zn^{2+}+In^{3+}+Sn^{4+}]$ ratio for a-$ZnIn_{8-x}Sn_xO_{13+0.5x}$ films on SiO_2/Si. (B) Threshold voltage (V_{th}) plots as a function of $[Zn^{2+}]/[Zn^{2+}+In^{3+}+Sn^{4+}]$ ratio for a-$Zn_{9-2x}In_xSn_xO_{9+1.5x}$ films on SiO_2/Si.

observed with SAND on increasing the Zn^{2+} content from $ZnIn_4Sn_4O_{15}$ to $Zn_3In_3Sn_3O_{13.5}$.

3.3.4. Threshhold Voltage (V_{th}) Dependence on Semiconductor Film Composition and Dielectric Type. Regardless of the dielectric type, an increase in threshold voltage is generally observed with increasing Sn^{4+} or Zn^{2+} content in the a-ZITO system. The high Sn content ($ZnInSn_7O_{16.5}$) gives $V_{th} = +63.7$ V and +1.8 V for films on the SiO_2 and SAND dielectrics, respectively; however, values of +27.4 V and +0.8 V, respectively, are observed for $ZnIn_7SnO_{13.5}$ films. For ZITO films with the Zn^{2+} composition increases identical to the Sn^{4+} content increases, a threshold voltage increase is also observed. For example, the threshold voltage of $Zn_7InSnO_{10.5}$ on SiO_2 is +79.9 V.

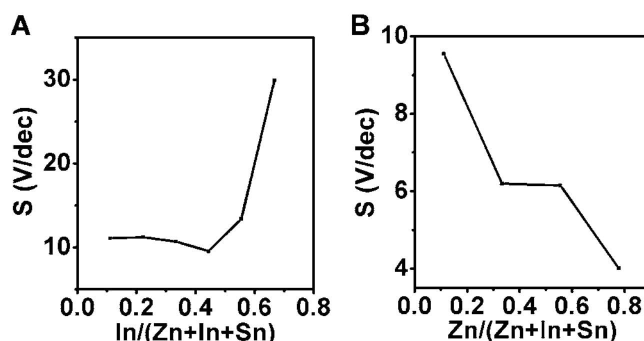

Figure 14. (A) Subthreshold swing (S) plots as a function of $[In^{3+}]/[Zn^{2+}+In^{3+}+Sn^{4+}]$ ratio for a-$ZnIn_{8-x}Sn_xO_{13+0.5x}$ films on SiO_2/Si. (B) Subthreshold swing (S) plots as a function of $[Zn^{2+}]/[Zn^{2+}+In^{3+}+Sn^{4+}]$ ratio for a-$Zn_{9-2x}In_xSn_xO_{9+1.5x}$ films on SiO_2/Si.

3.3.5. Subthreshold Swing (S) Dependence on ZITO Film Composition and Dielectric Identity. Subthreshold swing values are related to the density of interfacial surface states between the semiconductor and gate dielectric.[24] On SiO_2 and SAND, we observe similar S value trends. Thus, high In content $ZnIn_5Sn_3O_{14.5}$ films exhibit relatively large S values of 29.9 V/dec and 0.7 V/dec on SiO_2 and SAND, respectively. However, lower S values of 9.5 V/dec and 0.23 V/dec on SiO_2 and SAND, respectively, are measured for $ZnIn_4Sn_4O_{15}$ films. Furthermore, similarly low S values of 11.2 V/dec and 0.28 V/dec, respectively, are observed for Sn^{4+} composition increases up to $ZnInSn_7O_{16.5}$, while the increased Zn^{2+} content in $Zn_7InSnO_{10.5}$ depresses S to 4.0 V/dec on SiO_2 (Figure 14).

3.3.6. $ZnIn_4Sn_4O_{15}$ TFT Performance Dependence on Semiconductor Annealing Temperature. The optimized formulation $ZnIn_4Sn_4O_{15}$ was next chosen to analyze the effects of annealing temperature on TFT response. The device becomes TFT-active on annealing above 300 °C in air, and mobility significantly increases from 10^{-2} cm^2 V^{-1} s^{-1} to 11 cm^2 V^{-1} s^{-1} on increasing the annealing temperature from 300 to 400 °C. The current on/off ratio falls only slightly due to increased off-current with increasing annealing temperature, while the threshold voltage also falls with increasing annealing temperature. From the TFT performance dependence on annealing temperature shown in Figure 15, and the XPS results shown in Figures 5 and S3 (Supporting Information), it can be seen that annealing near 400 °C is required for essentially complete conversion of the metal oxide/hydroxide precursor into a metal oxide lattice and for oxygen vacancy generation.[13a]

3.3.7. Patterned $ZnIn_4Sn_4O_{15}$ TFT Performance. In the case of the unpatterned ZITO devices, some mobility overestimation

(26) (a) Torres-Delgado, G.; Zúñiga-Romero, C. I.; Jiménez-Sandoval, O.; Castanedo-Pérez, R.; Chao, B.; Jiménez-Sandoval, S. *Adv. Funct. Mater.* **2002**, *12*, 129. (b) Wang, A.; Babcock, J. R.; Edleman, N. L.; Metz, A. W.; Lane, M. A.; Asahi, R.; Dravid, V. P.; Kannewurf, C. R.; Freeman, A. J.; Marks, T. J. *Proc. Natl. Acad. Sci. U.S.A.* **2001**, *98*, 7113.

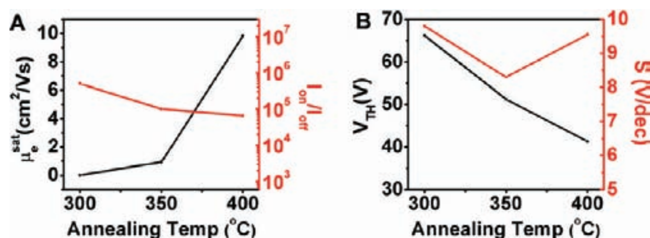

Figure 15. (A) Mobility and I_{on}/I_{off}, (B) threshold voltage (V_{th}) and subthreshold swing (S) dependence on annealing temperature for a-$ZnIn_4Sn_4O_{15}$ films on SiO_2/Si.

from peripheral currents is frequently unavoidable. Typically a ~10% mobility overestimation for W/L = 10 is observed in our studies[12b] and in the literature.[14] For a more accurate evaluation of field-effect mobility, we have also fabricated TFTs with patterned $ZnIn_4Sn_4O_{15}$ films (see Experimental Section for details) having 100 μm (L) × 5000 μm (W) contact geometries. The device performance obtained (Table 1) reveals electron mobilities of ~90 $cm^2\ V^{-1}\ s^{-1}$, which are comparable to those of the unpatterned devices. The on−off ratios are ~10^4−10^5, somewhat lower than those of the control devices, probably because of the enhanced leakage due to the extensive RIE processing. The V_{th} decreases to ~0.8 V, whereas S is unchanged at 0.22 V/dec.

4. Discussion

Figure 16 summarizes a-ZITO-based TFT performance metrics trends for the SiO_2 and SAND gate dielectrics as a function of ZITO film atomic composition. The proposed mechanism for electron transport in amorphous post-transition metal oxide semiconductors is based on percolation through highly dispersed spherical metal s-orbital states with additional 2p oxygen overlap.[7a,8a,26] Note that in field-effect devices, the gate-induced charges in the channel enable large carrier densities (>10^{19} cm^{-3}) which prefill trap sites. As a result, although in the off states these materials have lower carrier concentrations, larger field effect mobilities are possible, even larger than those obtained from Hall measurements.[4,5,27] Large cations such as In^{3+} and Sn^{4+} mediate electron transport through highly dispersed spherical metal s-orbital which extensively overlap as a consequence of their significantly larger expanse versus sp^3 O orbitals. For the present SiO_2-based ZITO devices, high field-effect electron mobilities are achieved by utilizing large s-orbital cation-rich compositions for significant orbital overlap, mixing In^{3+} and Sn^{4+} for structural relaxation, and further increasing structural relaxation via Zn^{2+} incorporation. In general, high temperature annealed In- or Sn-rich composition-based TFTs exhibit high off-currents and primarily negatively shifted V_{th} values due to the significant carrier concentrations and oxygen vacancies created by the high annealing temperatures, which are generally unavoidable in sol−gel precursor conversions.[7,13] In marked contrast, incorporation of small metal cations such as Zn^{2+} or Ga^{3+} lowers the off-currents because of suppressed oxygen vacancy formation that reduces the free carrier generation. This occurs because of the stronger metal−oxygen bonding of the small metal cations.[7a,6b,8a] The drawback, however, is that small metal cation incorporation generally depresses electron mobility, because the s−s orbital overlap is reduced for small cations.[7a,8a,26a] To minimize the effects of the small metal cation introduction, we chose Zn^{2+} which has a larger ionic radius than Ga^{3+} (6-coordinate radius = 0.74 Å for Zn^{2+} vs 0.62 Å for Ga^{3+}; 4-coordinate radius = 0.60 Å for Zn^{2+} vs 0.47 Å for Ga^{3+})[28] and therefore affords greater s-orbital overlap than does Ga^{3+}. This was the strategy here to investigate heavy metal mixing effects and stable dense phase formation in solution-processed ZITO films.

For crystalline ITO, a conventional transparent conducting oxide, the Sn^{4+} content is typically ~10 atom %, which maximizes the electrical conductivity by optimizing both the carrier concentration and mobility. It is known that when the Sn^{4+} content increases beyond this limit, the conductivity decreases due to the limited solubility of Sn^{4+} in In_2O_3, and formation of the poorly conducting $In_4Sn_3O_{12}$ phase.[20] In contrast, for TFT applications, high carrier mobility and *low* carrier concentrations are essential, and thus low carrier concentration phases are highly desirable. From the plotted data in Figures 9, 10, and 16, it can be seen that mixing In^{3+} and Sn^{4+} in a 1:1 atomic ratio as in a-$ZnIn_4Sn_4O_{15}$ films is effective at minimizing the off-current while retaining high mobility. From the field-effect mobility trends, it can be seen that the I_{off} current drop initially reflects a reduction in carrier concentration rather than a decline in mobility. The significant 10^4−10^5x decrease in carrier concentration from a-$ZnIn_7SnO_{13.5}$ to a-$ZnIn_4Sn_4O_{15}$ can be explained by assuming a local structural similarity of the amorphous phase to that of the corresponding crystalline phase and with similar Sn^{4+}−O^{2-} chemical bonding strength. Several studies have identified local structural similarities between amorphous TCO materials and the corresponding crystalline materials.[29] Since structure of crystalline $ZnIn_4Sn_4O_{15}$ films closely corresponds to that of $In_4Sn_3O_{12}$, structure(s) similar to that of the dense $In_4Sn_3O_{12}$ phase are also expected in amorphous $ZnIn_4Sn_4O_{15}$ films. Densely packed $In_4Sn_3O_{12}$ is an electrically neutral material and no doubt responsible for the significant drop in carrier density observed here.[20] The further 100-fold decrease in carrier density accompanying increased Sn^{4+} content from a-$ZnIn_4Sn_4O_{15}$ to a-$ZnInSn_7O_{16.5}$ can be rationalized by considering the stronger binding force between the highly charged Sn^{4+} and O^{2-}.

Interestingly, we observe the highest TFT mobilities when the In^{3+} and Sn^{4+} molar ratios are comparable within the a-$ZnIn_{8-x}Sn_xO_{13+0.5x}$ phase. The mobility of a semiconductor is typically proportional to the mean free scattering time and inversely proportional to the effective carrier mass. In general, impurity element inclusion in conventional covalent semiconductors increases scattering and lowers the mobility.[8a] However, both experimental and theoretical studies have argued that, for metal oxide semiconductors, compositional disorder does not significantly degrade electronic delocalization in the conduction band nor the resulting Hall mobility.[8a,30] The present mobility optimization by balancing the In^{3+}:Sn^{4+} ratio can be understood in terms of structural relaxation and densification effects. In Figure 13A, we observe minimum subthreshhold swing (S)

(27) (a) Nomura, K.; Kamiya, T.; Ohta, H.; Ueda, K.; Hirano, M.; Hosono, H. *Appl. Phys. Lett.* **2004**, *85*, 1993. (b) Takagia, A.; Nomura, K.; Ohta, H.; Yanagia, H.; Kamiya, T.; Hirano, M.; Hosonoa, H. *Thin Solid Films* **2005**, *486*, 38.
(28) (a) Shannon, R. D. *Acta Crystallogr.* **1976**, *A32*, 751. (b) Shannon, R. D.; Prewitt, C. T. *Acta Crystallogr.* **1969**, *B25*, 925.
(29) (a) Utsuno, F.; Inoue, H.; Shimane, Y.; Shibuya, T.; Yano, K.; Inoue, K.; Hirosawa, I.; Sato, M.; Honma, T. *Thin Solid Films* **2008**, *516*, 5818. (b) Nomura, K.; Kamiya, T.; Ohta, H.; Uruga, T.; Hirano, M.; Hosono, H. *Phys. Rev. B* **2007**, *75*, 035212. (c) Moriga, T.; Fukushima, A.; Tominari, Y.; Hosokawa, S.; Nakabayashi, I.; Tominaga, K. *J. Synchrotron Rad.* **2001**, *8*, 785.
(30) (a) Zhang, S. B.; Wei, S. H.; Zunger, A. *Phys. Rev. B* **2001**, *63*, 075205. (b) Robertson, J. *Phys. Rev. B* **1984**, *30*, 3520.

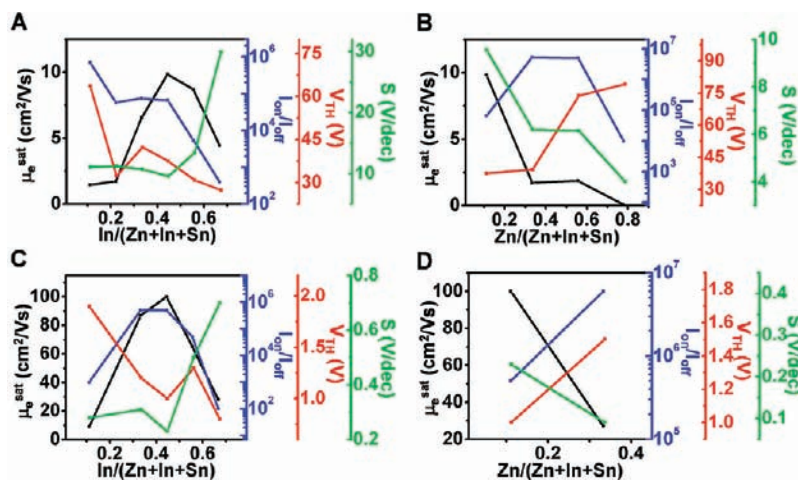

Figure 16. (A) Mobility, I_{on}/I_{off}, threshold voltage (V_{th}), and subthreshold swing (S) plotted as a function of $[In^{3+}]/[Zn^{2+}+In^{3+}+Sn^{4+}]$ ratio for a-$ZnIn_{8-x}Sn_xO_{13+0.5x}$ films on SiO_2/Si. (B) Mobility, I_{on}/I_{off}, threshold voltage (V_{th}), and subthreshold swing (S) as a function of $[Zn^{2+}]/[Zn^{2+}+In^{3+}+Sn^{4+}]$ ratio for a-$Zn_{9-2x}In_xSn_xO_{9+1.5x}$ films on SiO_2/Si. (C) Mobility, I_{on}/I_{off}, threshold voltage (V_{th}), and subthreshold swing (S) as a function of $[In^{3+}]/[Zn^{2+}+In^{3+}+Sn^{4+}]$ ratio for a-$ZnIn_{8-x}Sn_xO_{13+0.5x}$ films on SAND/Si. (D) Mobility, I_{on}/I_{off}, threshold voltage (V_{th}), and subthreshold swing (S) as a function of $[Zn^{2+}]/[Zn^{2+}+In^{3+}+Sn^{4+}]$ ratio for a-$Zn_{9-2x}In_xSn_xO_{9+1.5x}$ films on SAND/Si.

values and a mobility maximum at the $ZnIn_4Sn_4O_{15}$ composition within the a-$ZnIn_{8-x}Sn_xO_{13+0.5x}$ ($x = 1-7$) series. In ionic amorphous oxide transparent semiconductors, structural relaxation can generally be achieved by incorporating small corner-sharing tetrahedrally coordinating metal cations.[7a,c] Since small corner-sharing tetrahedra more flexibly engage in bonding with other octahedra and/or tetrahedra to relax structural distortion in amorphous matrices, due to their relatively isotropic nature, small cations stabilize the structure, decrease defect densities in the channel layer, and reduce subthreshhold swing values.[7a,c,31] The similar phenomenon observed here for In^{3+} and Sn^{4+} mixing suggests that mixing heavy metal ion octahedra is an effective way to reduce structural defects arising from distortion and to introduce structural stabilization. We suggest that the more relaxed size constraints and/or connection constraints provided by two different octahedra, not possible with In^{3+} or Sn^{4+} alone, can more easily accommodate structural fitting requirements. That is, diverse modalities for connecting heavy metal octahedra stabilize the structures of amorphous matrices with minimal bond angle distortions.

The dense $In_4Sn_3O_{12}$ structure has shorter average indium−oxygen distances than in bixbyite In_2O_3.[20] In amorphous matrices, the shorter metal−oxygen distances will result in shorter average metal−metal distances. Indeed, theoretical studies indicate smaller effective masses for dense rhombohedral In_2O_3 than for less dense bixbyite In_2O_3.[32] Smaller effective masses in dense phases can be readily understood in terms of increased overlap between conduction band metal s-orbitals due to the contracted average metal−metal distances. In the a-$ZnIn_4Sn_4O_{15}$ phase, increased s-orbital overlap between the heavy metal ions is expected from the dense packing, along with decreased electron effective mass and attendant increase in the electron mobility. However, further increases in the Sn^{4+} content, which should be accompanied by shorter metal−oxygen distances, apparently induce decreased s-orbital overlap instead, presumably due to the smaller Sn^{4+} ionic radius. In addition to the aforementioned heavy metal mixing effects, there is a substantial off-current decline on proceeding from conducting a-$In_4Sn_4O_{14}$ ($I_{off} > 10^{-3}$ A with 100 V bias for 100 μm length and 1000 μm length channels) to a-$ZnIn_4Sn_4O_{15}$, which likely reflects the strong oxygen binding of Zn^{2+}. As is evident in Figure 16B, further increases in the Zn^{2+} content depress the mobility and subthreshhold swings of the resulting TFT devices.

As explained above, a compositionally balanced, mixed heavy metal oxide system with minimal Zn^{2+} incorporation provides significant intrinsic electron mobility, however the fabricated devices still exhibit only moderate field effect mobilities of ~10 $cm^2\ V^{-1}\ s^{-1}$ on Si/SiO_2 dielectric layers, even after high temperature annealing. It is known that by choosing the proper gate dielectric, the field-effect mobility of many semiconductors is substantially increased due to, among other factors, reduced interface trap densities[3c,4,33] Previously, our group demonstrated that thermally robust ultrathin, high-capacitance SAND affords significantly enhanced TFT performance when combined with a variety of semiconductors, including metal oxide films and nanowires.[3f,12b,25] Furthermore, SAND enables low operating voltages due to the high capacitance. From the transfer and output plots in Figures 7C,D and 10, optimized a-$ZnIn_4Sn_4O_{15}$ films on SAND exhibit impressive electron mobilities of ~100 $cm^2\ V^{-1}\ s^{-1}$ for unpatterned devices ($W/L = 10$) and ~90 $cm^2\ V^{-1}\ s^{-1}$ for patterned devices ($W/L = 50$). The maximum values we obtain are 113 $cm^2\ V^{-1}\ s^{-1}$ for the unpatterned devices and 104 $cm^2\ V^{-1}\ s^{-1}$ for patterned devices. The corresponding I_{on}/I_{off} ratios are $\gtrsim 10^5$ for the unpatterned devices and $\gtrsim 10^4$ for patterned devices. The decrease of I_{on}/I_{off} ratio of the patterned devices is reasonably attributed to increases in off-current due to RIE effects in the patterning process. Note that these TFT metrics are comparable to those of many single-crystalline or large-grain polycrystalline Si devices.[34] Moreover, a-$ZnIn_4Sn_4O_{15}$ based devices on SAND gate dielectrics exhibit almost hysteresis-free response and minimal trapped charge,

(31) Narushima, S.; Mizoguchi, H.; Shimizu, K.; Ueda, K.; Ohta, H.; Hirano, M.; Kamiya, T.; Hosono, H. *Adv. Mater.* **2003**, *15*, 1409.
(32) Karazhanov, S. Z.; Ravindran, P.; Vajeeston, P.; Ulyashin, A.; Finstad, T. G.; Fjellvåg, H. *Phys. Rev. B* **2007**, *76*, 075129.
(33) (a) Seon, J.-B.; Lee, S.; Kim, J. M.; Jeong, H.-D. *Chem. Mater.* **2009**, *21*, 604. (b) Cui, Y.; Zhong, Z.; Wang, D.; Wang, W. U.; Lieber, C. M. *Nano Lett.* **2003**, *3*, 149.
(34) (a) Khang, D.-Y.; Jiang, H.; Huang, Y.; Rogers, J. A. *Science* **2006**, *311*, 208. (b) Shimoda, T.; Matsuki, Y.; Furusawa, M.; Aoki, T.; Yudasaka, I.; Tanaka, H.; Iwasawa, H.; Wang, D.; Miyasaka, M.; Takeuchi, Y. *Nature* **2006**, *440*, 783.

unlike the analogous SiO_2-based devices. Also from the data in Table 2, note that the calculated values of D_{it} from the S data indicate that there is a significant decrease in trap density on changing to the self-assembled gate dielectric. The large mobility enhancement of ~10x going from SiO_2 to SAND can be attributed principally to interface improvements.[3f,33] Indeed, low-frequency noise measurements show that SAND gate dielectrics can provide a significant trap site reduction versus SiO_2.[35] This may reflect the softer SAND interface. We speculate that in the present case, SAND may better accommodate the formation of the semiconductor metal oxide lattice upon thermally induced precursor decomposition. We also speculate that the softer SAND surface may relax mechanical stress at the dielectric−semiconductor interface upon oxide lattice formation, thereby providing a more regular semiconductor−dielectric interface.

Conclusions

Solution-processed amorphous metal oxide thin films having high In and Sn contents provide greater TFT electron mobilities than previously reported oxide thin films having low In and Sn contents, by introducing structural relaxation and trap density reduction mechanisms along with minimal small cation stabilizer incorporation. On a 300 nm SiO_2 dielectric, Zn-rich $Zn_7InSnO_{10.5}$ ($\mu_e^{sat} \approx 0.06$ cm^2 V^{-1} s^{-1}), Sn-rich $ZnInSn_7O_{16.5}$ ($\mu_e^{sat} \approx 1.4$ cm^2 V^{-1} s^{-1}) and In-rich $ZnIn_6Sn_2O_{14}$ ($\mu_e^{sat} \approx 4.4$ cm^2 V^{-1} s^{-1})-based TFTs exhibit modest mobilities compared to $ZnIn_4Sn_4O_{15}$-based devices ($\mu_e^{sat} \approx 11.4$ cm^2 V^{-1} s^{-1}). Furthermore, the current on/off ratio is significantly degraded in In-rich $ZnIn_6Sn_2O_{14}$ ($I_{on}/I_{off} \approx 10^2$) due to the high off-current. With properly balanced multicomponent heavy metal-rich oxide systems, enhanced field-effect mobilities and current on/off ratios, up to 11.4 cm^2 V^{-1} s^{-1} and 10^4−10^5, respectively, are observed on 300 nm SiO_2 gate dielectrics. Moreover, with optimized dielectric−semiconductor interfaces, the solution-processed metal oxide device performance is enhanced to levels comparable to vacuum-deposited polysilicon or optimized metal oxide films. Furthermore, the present TFTs operate at very low voltages (<3 V). These results are encouraging for developing large area, high-speed, low-power applications.

(35) (a) Ju, S.; Kim, S.; Mohammadi, S.; Janes, D. B.; Ha, Y.-G.; Facchetti, A.; Marks, T. J. *Appl. Phys. Lett.* **2008**, *92*, 022104. (b) Ju, S.; Chen, P.; Zhou, C.; Ha, Y.-G.; Facchetti, A.; Marks, T. J.; Kim, S. K.; Mohammadi, S.; Janes, D. B. *Appl. Phys. Lett.* **2008**, *92*, 022104.

Acknowledgment. The research was supported by the MRSEC program of NSF (DMR-0520513) at the Northwestern University Materials Research Center and by AFOSR (FA9550-08-1-0331). Microscopy; XPS studies were performed in the EPIC, NIFTI, KECK-II facilities of NUANCE Center at Northwestern University. NUANCE Center is supported by NSF-NSEC, NSF-MRSEC, Keck Foundation, the State of Illinois, and Northwestern University.

Supporting Information Available: AFM images, transfer plot and output plot, UV−vis spectra, Table S1 and Figures S1−S5, and complete ref 1c. This material is available free of charge via the Internet at http://pubs.acs.org.

JA100615R